



# INTRALAB MEMORANDUM

To: Distribution  
From: Joe Paradiso  
Date: 20-March-1991  
Subject: **Electronics for Testing the Wideband Monopulse Sensor**  
Memo #: EJB 91-029

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## **Abstract**

This memo outlines the circuitry that has been designed and constructed/tested to support a channel of the PVF2 monopulse "backgammon" sensor. The analog front-end is first described, along with the sum, difference, and integration functions needed to produce the pair of signals that encode the bearing. A circuit is also described that samples this pair coincidentally (at the peak value of the denominator signal over an adjustable gate range), and takes an analog ratio to yield a voltage that is proportional to the directional cosine of the incident angle. These circuits are needed for the upcoming underwater tests of the prototype sensors. Suggestions for design improvements are liberally sprinkled throughout the text.

## 1) Front-End and Analog Processing

The front-end analog circuitry used to buffer and amplify the raw monopulse signals is given at the bottom of Fig. 1. There are six of these circuits; one dedicated to each of the six sensor stripes. The common foil deposited on the PVF2 ("CC") is grounded, together with an insulated ground plane behind the pickup electrodes (1A-2C). The potential between this ground and the pickup electrodes (1A-2C) yields the raw sensor signal. The JFET and resistors to the left of the dotted line are located on the back of the sensor itself. Because of the small ( $\leq 30$  mV), high-impedance sensor signals, significant problems can be encountered with noise and extraneous (i.e. 60 Hz) pickup; the JFET source follower was added as a local buffer to drive a cable out of the sensor with a lower impedance. The 1 Meg resistor at the gate of the JFET bleeds off long-term charge on the sensor and provides a bias to drive the FET. This resistor could be made higher, extending the bandwidth of the sensor into the sub-hertz range. As the frequencies of operation are anticipated to be well above this (and the noise at low frequencies due to mechanical stress can be overwhelming), this resistance (originally at 30 Meg) was dropped to roll off the extreme low end. Provided that the sensor impedance is sufficiently low at operating frequencies (i.e. beyond 50 KHz), this 1 meg should be fine; if the sensor impedance remains up at the hundreds of  $K\Omega$ , however, the tolerance of this resistor will significantly affect the magnitude of the transmitted signal. In addition, the voltage gain of the JFET is slightly less than unity, and can vary device-to-device. The source-follower gain can be described as  $\mu/(\mu+1)$ , where  $\mu = g_m r_d$ , both of which are device parameters, and can vary between packages. Ideally,  $\mu$  is very large, and a limited uncertainty in its magnitude will not propagate appreciably into the voltage gain. This will have to be examined in detail when production units are designed; FETs with  $\mu$  sufficiently large and uniform will be needed to maintain precision. Other configurations are possible; i.e. with somewhat more real-estate, one can place an OP-amp circuit on the sensor that can also provide a precise voltage gain, which may be needed if one desires to drive a long, terminated cable with a limited signal. The source follower, however, is a minimum-component solution (the 11K source resistor can be placed away from the sensor, at the other side of the coax, and only one  $0.1 \mu$  capacitor is needed per 3 sensor electrodes). It can be readily constructed with surface-mount components placed directly on the edges of the sensor. The 2N3819 was chosen primarily because of its ready availability (i.e. at the Radio Shack). Although it is probably adequate here, other FETs should also be examined for superior performance in noise, gain variation, SOT-23 availability, etc. before any particular device is adopted for "production" models.

At the other end of the coax (i.e. above water), the signals are decoupled with  $0.1 \mu$  capacitors into a 10 K load, providing additional attenuation of the low-end (rolling off at 160 Hz). The operational frequencies (i.e. 50 - 200 KHz) are significantly low to allow omission of the  $50-75\Omega$  cable termination for the short cable lengths used in these tests. Amplifier A8 will yield a precision gain of 10 (getting more out of these TLO82-class OP-Amps is not recommended,

particularly for eventual operation near 200 KHz). It's structured as a non-inverting amplifier, since it dates from a prototype without the source followers (thus A8 was the front-end, and needed a high impedance input). With the introduction of the JFET's, the high impedance is no longer required, and A8 could be an inverting amplifier. Better noise performance may also be achieved by going to a low-noise bipolar amplifier for A8 (i.e. the 5534 or 5532).

Amplifier A9 is configured as a Sallen-Key second-order highpass filter with a 3 dB cutoff at 2.4 KHz and a passband gain of 2.2. This is inserted to pull out most remaining noise due to mechanical deformation, low-frequency external pickup, and environmental sound. The sensor is planned to be operated at frequencies well above this cutoff, thus this filter should introduce negligible effect in the sensor performance. Two outputs are provided; one to the outside world (for external data collection of all subapertures), and another to the processing electronics depicted at the top of Fig. 1. These signals will still be fairly small (i.e. probably 500 mV or less), but probably adequate for data collection systems. No rolloff of the high-end was provided in this front-end circuitry, beyond the intrinsic bandwidth of the OP-amps (which will kick in beyond 200 KHz). If high-frequency noise becomes a problem, a small feedback capacitor could be added to A8, and/or rolloff could be imposed at the output of A9. This was not needed for the current tests, however, thus such capacitors were not included to enable operation at high frequency.

The top portion of Fig. 1 shows how the sensor subaperture signals are processed to form the pair whose relative scaling encodes the direction cosine of incident angle. A1 and A3 precisely sum subapertures in the left and right sensor halves. These are subtracted in A4, then integrated in A6 (to recover the phase and frequency-dependent scaling), and boosted in A7. Substantial additional gain is added in this circuit by each stage, resulting in a hefty signal at the N (numerator) output. The signal level may be adjusted by the "N Gain" trimpot before the integrator (where the signal should still be far from saturation). The integrator is realized as a lowpass filter with 3 dB rolloff ( $-45^\circ$  phase) at 1.6 KHz. This yields  $-84^\circ$  phase at 16 KHz and  $-88.5^\circ$  phase at 60 KHz, where we'll operate in our tests. If additional phase shift is desired, the time constant in the integrator A6 can be readily decreased by increasing the values of the feedback components.

The two linearly-tapered subapertures are precision-summed in A2, and boosted an order of magnitude in A5, producing the denominator (D) output. The gain of this signal is adjusted by a trimpot in the feedback of A2.

The accuracy of the sums taken in these circuits are affected by the precision of the (\*) superscript resistors, in addition to the device-to-device variance between front-end source followers, as discussed earlier. The present circuit uses 1% resistors (available in our stockroom) for the (\*) values, and 0.1% components or better (which need to be ordered) can readily be substituted in future designs. Errors can easily be propagated through the linear circuitry here, yielding the component tolerance needed to guarantee a result of required precision. In order to calibrate the front-end gains of the presently-built prototype, a small fixed signal can be injected at the gates of the 2N3819's, and the response at the output of A9 can be measured (this can provide

corrections to the off-line analysis performed on the sampled 1A-2C outputs). The accuracy of the N and D signals otherwise arise from the resistor tolerances in the sum and difference amplifiers A1-A4.

## 2) Gated Peak-Demoninator Ratio Generator

This simple circuit, shown in Fig. 2, was designed in order to obtain a very quick approximate indication of the sensor performance in estimating bearing, without requiring digital sampling or off-line analysis. It accepts the N and D signals output from the analog conditioning circuitry of Fig. 1. Both of these signals are simultaneously sampled and latched at the peak positive value of the denominator (D) signal that is encountered during an adjustable gate interval after the receipt of a trigger input. An analog divider takes the ratio of these voltages (N/D), and provides outputs that can drive a meter or otherwise provide a display that is (ideally) proportional to the direction cosine of the incident wavefront. By latching both signals at the time of the peak denominator value, the noise sensitivity is minimized (noise can contribute significantly to a ratio formed with a small denominator). An adjustable gate is provided that allows one to set the length of the active interval that follows receipt of a trigger input; this gate will be set sufficiently narrow for the sampler to respond only to the primary source sound paths, and not later reflected arrivals.

A quick summary of the design can be made by referencing Fig. 2. The N and D inputs are latched simultaneously by the AD 682 dual sample/hold (outputs of these latched signals are made available off-card for diagnostic purposes). The ratio of the latched signals, N/D, is then taken by the AD 633 multiplier, which is in feedback around A3. The remainder of the circuitry determines when the N and D inputs are latched; i.e. at the peak value of D during the gated interval. The sample gate is determined by comparator K1, which compares the D input to the sample/hold D output. If the D input is significantly greater than the sample/hold D output, K1 goes low, forcing the collector of Q2 high, and opening the sample gate, allowing the sample/hold outputs to track the inputs. Comparator K1 is enabled (i.e. allowed to go low) only when transistor Q1 is off. This occurs when the slope of the D input is positive and the gate is high or the free run switch is closed. In this fashion, K1 is forced high when the signal begins to decrease or the gate ends, latching both N and D into the sample/hold. This will result in both N and D signals to be sampled at the point where D had its maximum positive excursion during the gated interval.

The slope of the D input is taken by differentiator A2 (buffered by follower A1). The sign of this slope is determined by the comparator K2 (the 510 K feedback provides a minimal hysteresis to aid in stability). A measure of hysteresis was also introduced into K1 via the 300 K resistor to the collector of Q2. This prevents a "walk-down" effect, where a slowly decreasing D input amplitude will cause K1 to fire (and samples to be taken) at the peak of every cycle. The hysteresis will cause K1 to fire only if the D input is significantly higher than the sampled D output. The contributions of "spikes" in the sample-hold output to spurious firing (and this "walk-down" effect) are

reduced by including the 100 pf shunt capacitor at the noninverting input of K1 (this effect of this on the D signal is balanced by a similar network at the N input). This effectively limits the operation of the circuit to D signals under 100 Khz; if one desires to run with faster inputs, this capacitor should be reduced or eliminated.

The gate is generated by a monostable in the 74123 package. A TTL rising edge at the "Trigger" input (or a press of the "Manual Trigger" button) will produce a brief (i.e.  $< 1 \mu\text{sec}$ ) pulse from one of the monostables (labeled RS) in the package. This pulse forces a sample to be taken by pulling down the base of Q2, thereby initializing the sample/hold with the N and D inputs. The RS pulse also triggers the other monostable in the 74123, producing the actual gate. The gate width can be adjusted through a dedicated potentiometer on the circuit card. The gate signal is brought off-card to facilitate triggering and width adjustments during sensor testing. The "free run" switch essentially produces a valid gate while it is closed, causing the sample/hold to continuously track the peak value of the D signal.

This circuit has been designed only to provide an approximate aid in test procedures, and not with a precision measurement in mind. It seems to work fairly well, however. One potential source of inaccuracy is in the occasionally narrow sampling gate driving the AD682. This should be over 900 nsec. It can be somewhat less, however, potentially introducing limited error after some trigger inputs. At the risk of limiting input bandwidth, it can be made to be a minimum of 900 nsec (i.e. OR the Q1 output with a monostable triggered by K1), which may produce more stable values. This problem doesn't seem too significant in the current design, thus the above "fix" isn't included at the present time.

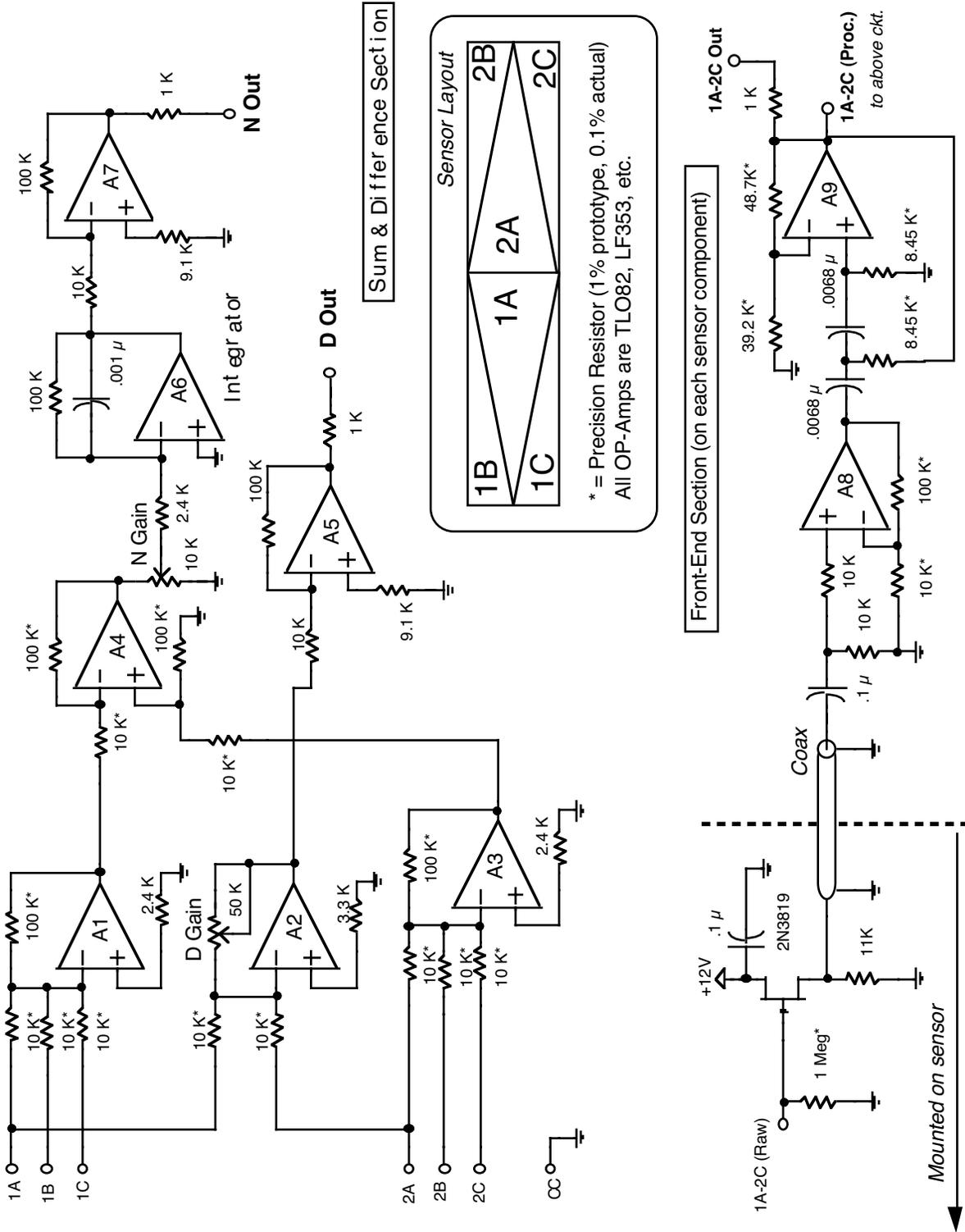


Figure 1: Analog Front-End and Signal Conditioning

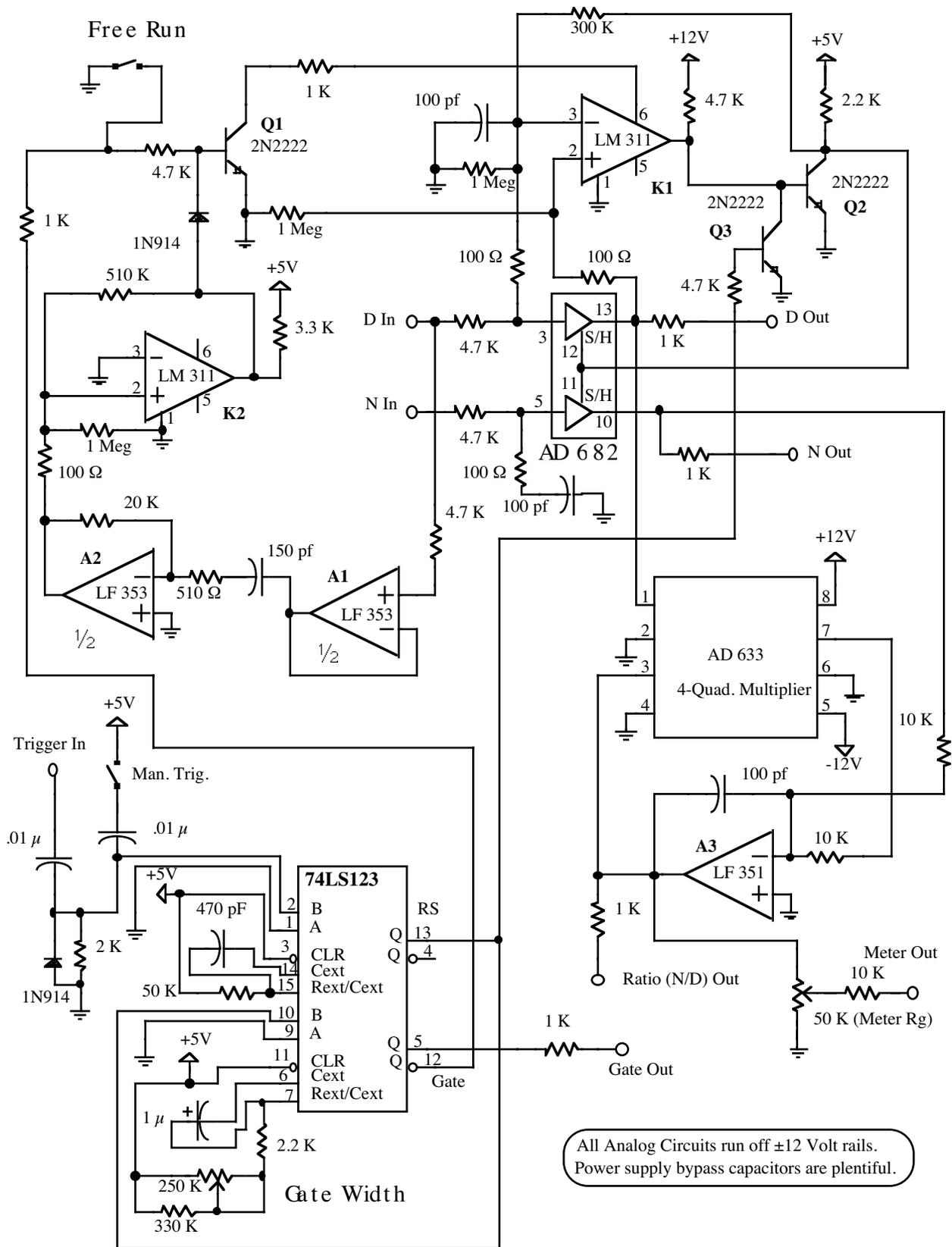


Figure 2: Gated Peak Denominator Ratio Generator (Bearing Estimator)