# INTRALAB MEMORANDUM

To: Distribution

From: Joe Paradiso

Date: 13-October-1991

Subject: **Backgammon Electronics; Past, Present, & Future**

Memo #: EJC 91-1100

Copies:


## Abstract

This memo elucidates the changes that have been made over the past months in the electronics used to amplify and process signals from the PVDF "Backgammon" monopulse sonar system. A new front-end amplifier system is currently under construction; its design is introduced and discussed.

**1) Past & Present**

During the spring and summer of 1991, the prototype Backgammon sensor stave has been frequently tested in Boston Harbor. The experience attained in these tests has resulted in several small changes to the sensor electronics (as were originally baselined in my memo of 20-March-1991, "Electronics for Testing the Wideband Monopulse Sensor", EJB 91-029). While most of the circuitry discussed in that memo remains relevant, significant changes have been made. The updated schematics are appended to this report.

The first schematic shows the changes made to the analog front-end and signal conditioning electronics. One may compare this to Figure 1 of EJB 91-029 in order to note the differences. An RC line filter has been added to the DC supply driving the JFET source followers placed on the sensor stave; this reduces any low-frequency noise or ripple/hum that is injected into the input signal via the power supply. In order to further reduce pick-up noise, the topside front-end amplifier has been changed into a differential line receiver. Because of the relatively high output impedance of the JFET source followers (i.e. around 2 KΩ), the sensor-to-topside line can't be terminated too aggressively; 10 KΩ termination resistors are currently used (more on this later in Sec. 2).

The integrator in the Sum and Difference Section has been replaced by an adjustable all-pass filter. The integrator was seen to roll off the sensor signal too aggressively at frequencies beyond 15 Khz, thus caused a noisy response at most frequencies of interest. Since our tests will be primarily narrowband, there is no need for this integrator; the all-pass filter that replaces it can be adjusted to yield a 90° phase shift (or match the denominator (D) and numerator (N) signal phases) at the desired test frequency, while retaining full signal amplitude at all frequencies, and thus achieve superior noise performance. An additional gain block has been inserted before the unity-gain all-pass filter in order to substitute for the gain that had been contributed by the integrator.

If a wider-band response is desired, one can go back to the original design, and re-insert the integrator (with a time constant, however, that is better matched to the frequencies of interest), or introduce a differentiator into the denominator ("D") output. At this stage, however, these operations may be better accomplished through a Digital Signal Processing (DSP) system (which is readily adaptable), rather than continuing to pursue an analog design.

An additional "Pre-Integrator" output has been provided, in order to allow an external tap into the "N" signal before it is processed by the phase shifter (thus this signal can be monitored, digitized, stored, and [if desired] integrated off line). The trimpots to adjust the D gain, N gain, and phase shift are labeled on the card by a handwritten "D", "N", and "P" respectively.

All sensor signals are picked-off before they are filtered in the 3 Khz high-pass circuit of A11, then routed to an audio amplifier and trigger circuit depicted in the next schematic. These signals are separately summed into left/right groups (referring to the sensor sides; A12 sums one side, A13 sums the other), then combined together. One of the sides may be inverted with respect to the other by flipping an on-board toggle switch. This alters the amount of common-mode signal that

is passed, and similarly changes the perceived sensor response. This signal sum is provided as an audio tap via a standard RCA jack; it can be used for monitoring (all other sensor outputs have a 3 Khz highpass response) or recording. The audio sum is also amplified by a LM386 audio amplifier, which is routed to a standard ¼" stereo headphone phone jack. This provides an invaluable diagnostic aid; one can readily monitor sensor performance (i.e. by listening to boats, dolphins, and ambient underwater sound sources), plus receive immediate guidance on reducing sources of AC hum, pickup, etc. As the gain in this circuit is relatively high, and the sensor noise is fairly low, one must be cautious while using headphones; abrupt sound sources (such as dropping a penny on the topside barge) can be painfully loud, thus use the onboard volume trimpot (labeled with a "V" on the card) judiciously.

This circuit also contains an adjustable discriminator, which can be used to trigger the peak/ratio sampling gate (or an external DAS system) on high-amplitude transient signals (thus one can trigger on ambient sound sources). The threshold of this discriminator can be tuned via an on-card trimpot (labeled with a "T"); an on-card LED is also provided as a discriminator monitor (the discriminator output is stretched via a diode-capacitor network in order to provide a visible indication of brief signals). The discriminator output runs 0 → 5 Volts, and is TTL-compatible.

The next schematic shows the current version of the Peak Denominator Ratio Generator. This circuit hasn't changed too much from the version that was shown in EJB 91-029. An on-card LED has been provided to monitor the gate output; this helps in setting input triggers and gate widths. A range switch has been added on the circuit card to extend the possible gate widths. With this switch off (always the case with the former design), the gate can be widened only up to 40 msec. With the switch on, the gate can attain widths approaching 600 msec (which spans the time required for sound to transit the length of water beneath the test barge). The wiring around the 74123 has also been slightly altered so that the peak/ratio generator can not be re-initialized after the gate is active. With this new wiring, the circuit will find the ratio corresponding to the largest denominator amplitude over the entire gate width. Additional trigger signals that arrive during the gated interval will not reset the peak/ratio generator (as was the case previously).

The modifications sketched above have already been incorporated into the existing backgammon electronics. Test results have been very promising; noise and pickup levels have been reduced to insignificant levels, and the sonar source is seen to produce good signals at the sensor stave on the opposite side of the barge. The last wet test that was performed showed an angular resolution that appeared to be within a degree, but couldn't be better determined because of signal/noise loss introduced by the integrator that was still in the signal conditioning electronics. The replacement of the integrator with the all-pass phase shifter should aptly remove this difficulty. Unfortunately, tests with the phase shifter have been delayed, due to restricted barge access (i.e. the summer ferry schedule), and water leakage through the ScotchCoat™ protection on the sensor stave electronics and cable splices. These difficulties have been remedied, and testing will resume shortly,

with detailed results forthcoming.

**2) The Future....**

The electronics developed thusfar are adequate for the impending tests, and should be able to provide good proof-of-concept measurements. A new generation amplifier has been designed, however, which should provide superior signal/noise performance, and should be adequate for a deployed system. This amplifier will provide a factor of 23 voltage gain at the sensor stave, and be able to drive a 600 Ω balanced line to the topside electronics.

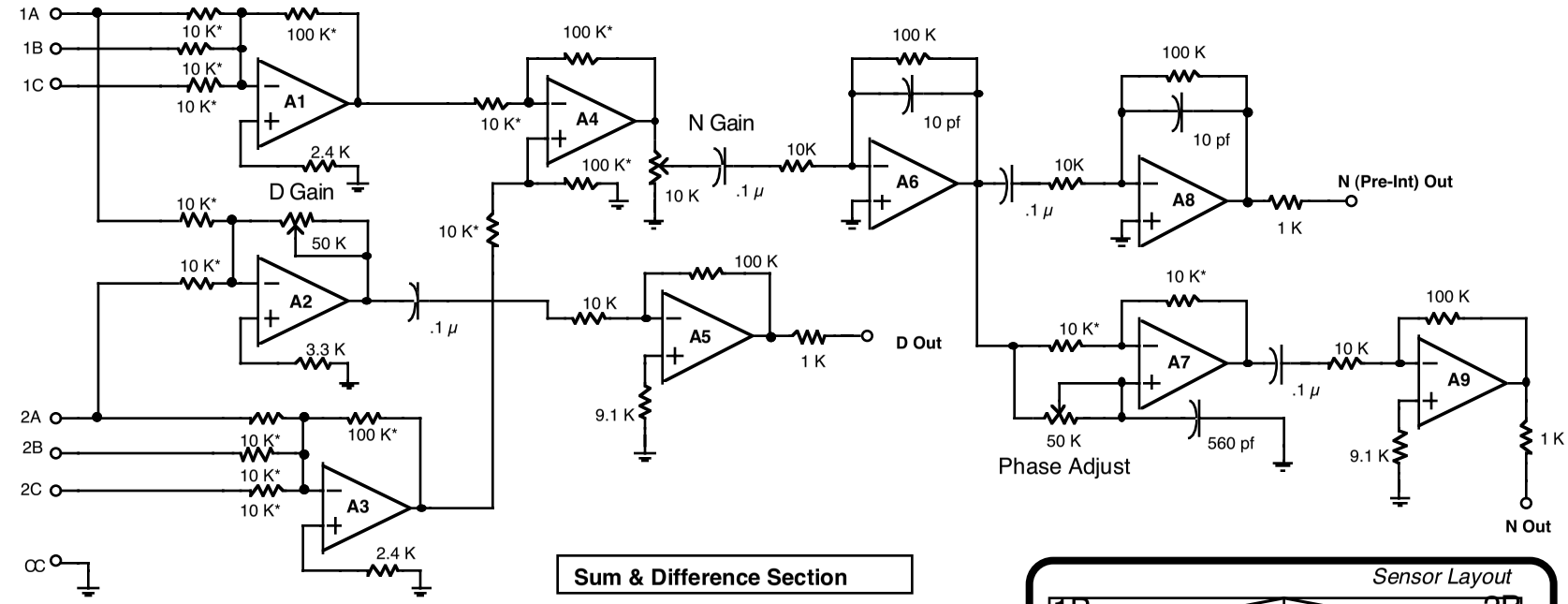
The schematic is appended to this document. It is based around a new low-noise JFET OP-AMP from Analog Devices, the AD745. It has been designed with sonar systems in mind, and the front-end has been adapted from their application suggestions. The front-end device is configured as a non-inverting high-pass filter, with time constant determined by the 1K resistor and 0.68 $\mu$F capacitor (here producing a cutoff at 230 Hz, removing low-frequency thermal and mechanical noise). Any DC bias floating across the sensor is removed by the 100 Meg parallel resistor. An optional integration feedback capacitor can be added, if needed, to the front-end amplifier to reduce the high-end frequency response and introduce additional stability.

The second-stage unity-gain differential line driver (the SSM 2141) is capable of putting several volts into a 600 Ω balanced line, which is terminated at the topside signal conditioner. The topside termination is currently set at 10 KΩ (for the high-impedance JFET drivers now being used); this may be dropped to 600 Ω after these amplifiers are introduced, yielding better pickup rejection. In addition, future topside analog electronics can be built around the companion SSM 2142 line receiver, rather than the discrete circuitry built around a differential-input OP-AMP (A10 in the conditioner schematic); this may be more convenient, and yield even better common-mode rejection due to better component tolerances.

A PC layout has been made for this amplifier, as appended to this report. These are 3-channel cards. Two of them will easily fit within the 1 7/8" wide sealed cavity that has been designed behind the sensor stave (this should remedy the leaking ScotchCoat problem once and for all...). Smaller dimensions can readily be attained by using surface-mount components. A bundle of twisted pairs has been procured in a shielded underwater-qualified cable (vs. the discrete single-line shielded cable bundle currently used). The underwater cable shield will be grounded both topside and at the sensor stave. If this produces ground loop and pickup problems, the shield can readily be floated from the sensor stave ground (this connection is made through removable straps on the amplifier circuit cards).

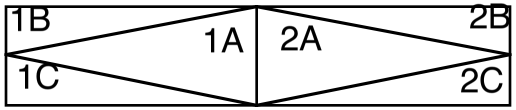
The sensor pickup electrodes will now be sandwiched between two ground planes; one provided by the PVDF conductive backing, and the other provided by a copper-clad G10 strip placed behind the pickup electrodes (the present sensors lack this latter strip). This should improve the sensor shielding considerably.

The minimal electronics requirement at the sensor location was provided by the JFET source follower that is currently in use. Since this isn't the best solution for the sonar sensor (i.e. relatively high output impedance, no voltage gain), it is being replaced by the dual stage design discussed in this section. The JFET does still have application, however, in situations that place restrictions on the amount of electronics that can be introduced at the sensor location (i.e. in the related "Center of Pressure" sensor). In this case, microchip (i.e. "flea-sized") JFET devices can be mounted directly on the sensor foils, providing a moderate-impedance cable drive, with minimum perturbation on the "flatness" of the physical sensor.



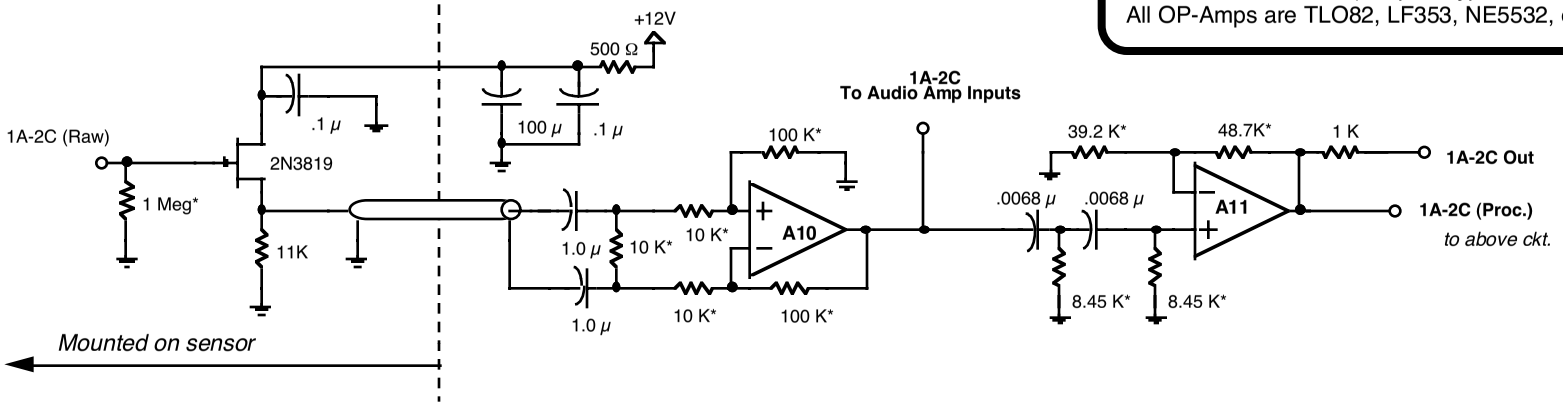

**Sum & Difference Section**

*Sensor Layout*

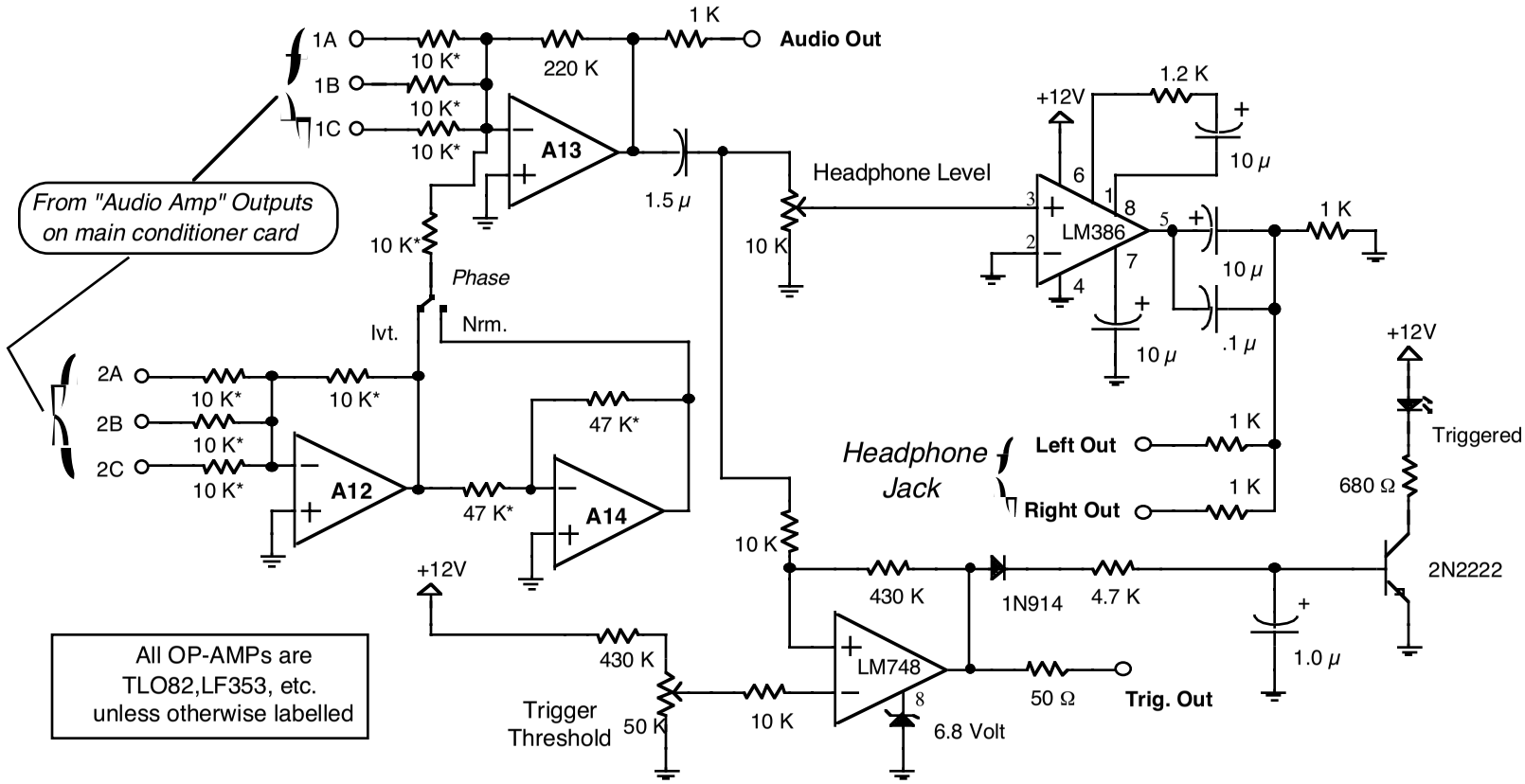



* = Precision Resistor (1% prototype, 0.1% actual)
All OP-Amps are TLO82, LF353, NE5532, etc.

Front-End Section (on each sensor component)

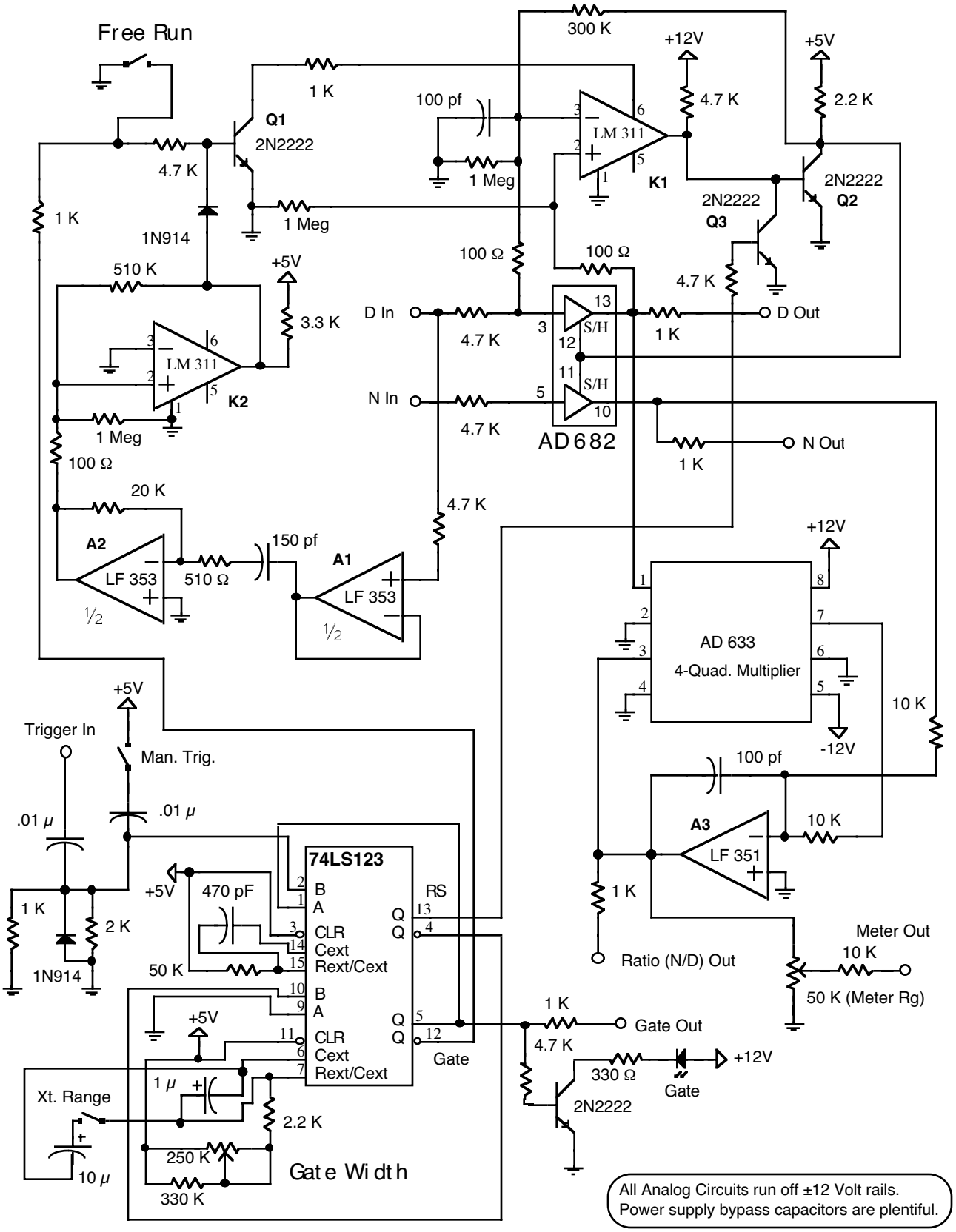



# Analog Front-End and Signal Conditioning (October, 1991)

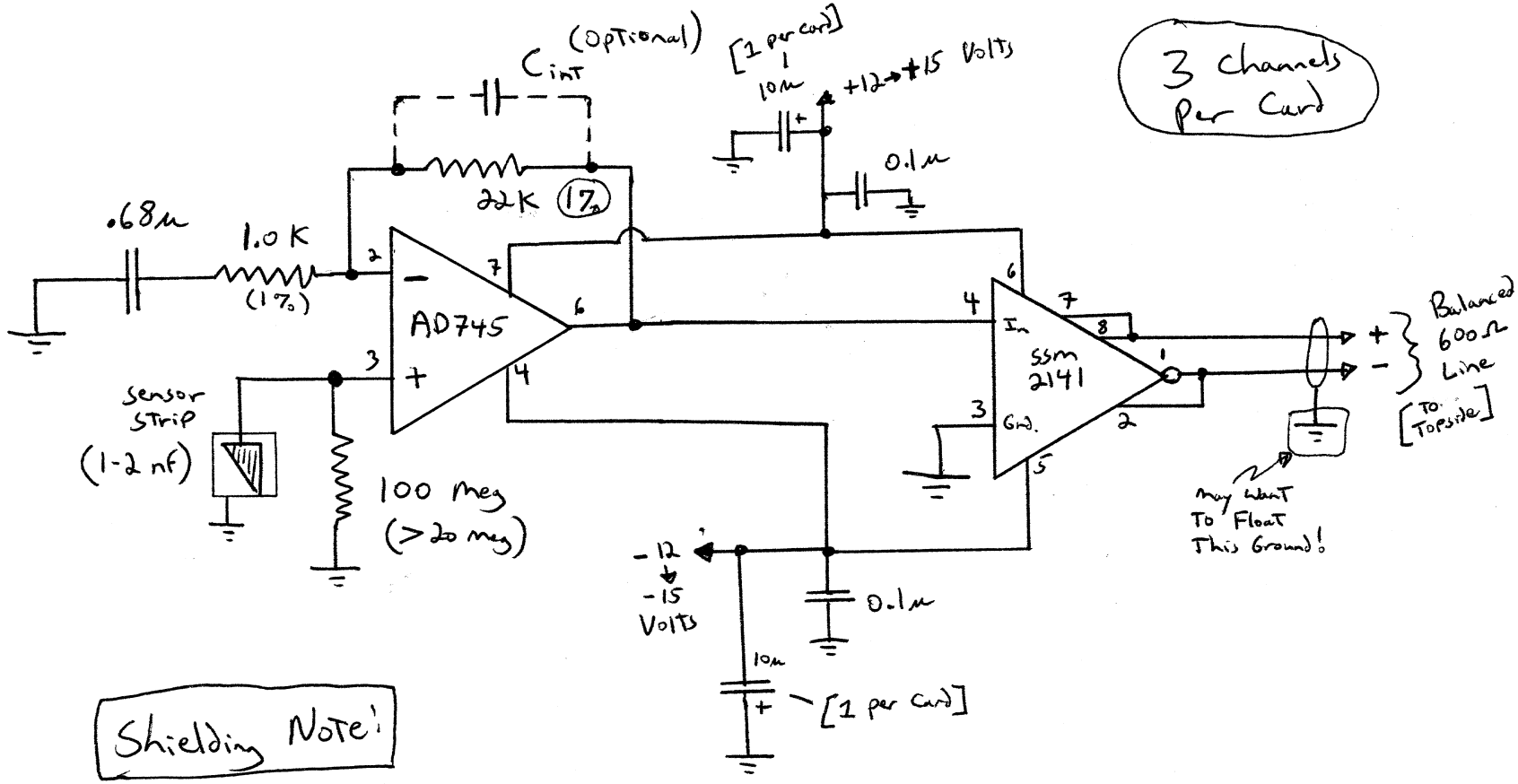



# Headphone Monitor Amplifier & Amplitude Discriminator

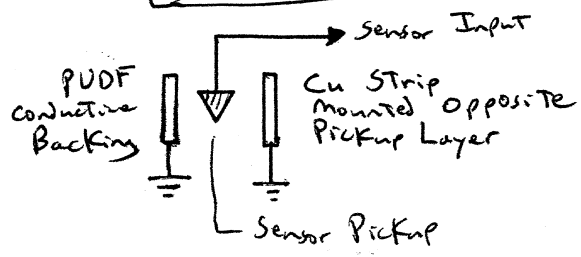
## Gated Peak Denominator Ratio Generator (October, 1991)



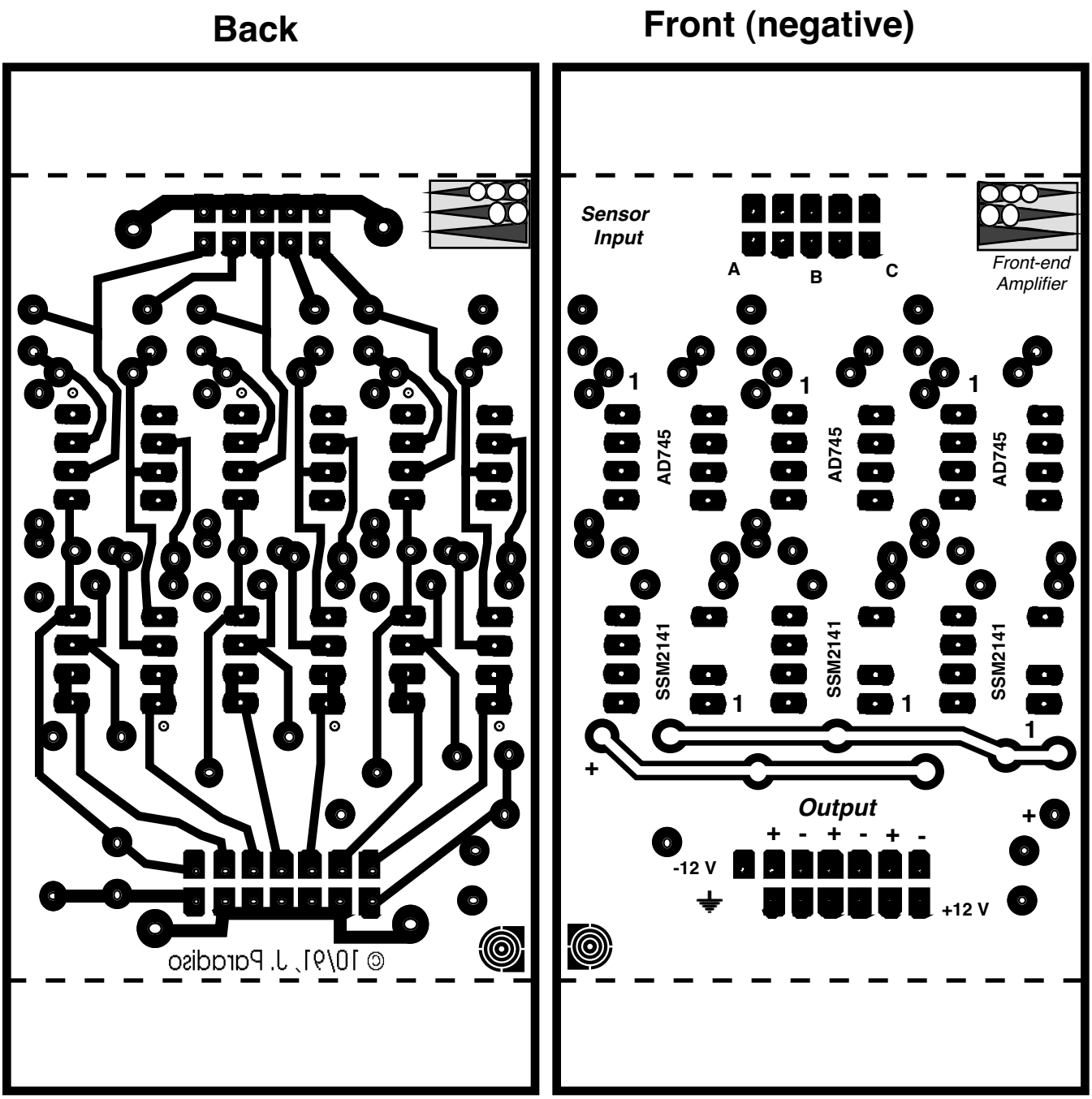
# Improved PVDF Front-End Amplifier




## Shielding Note:



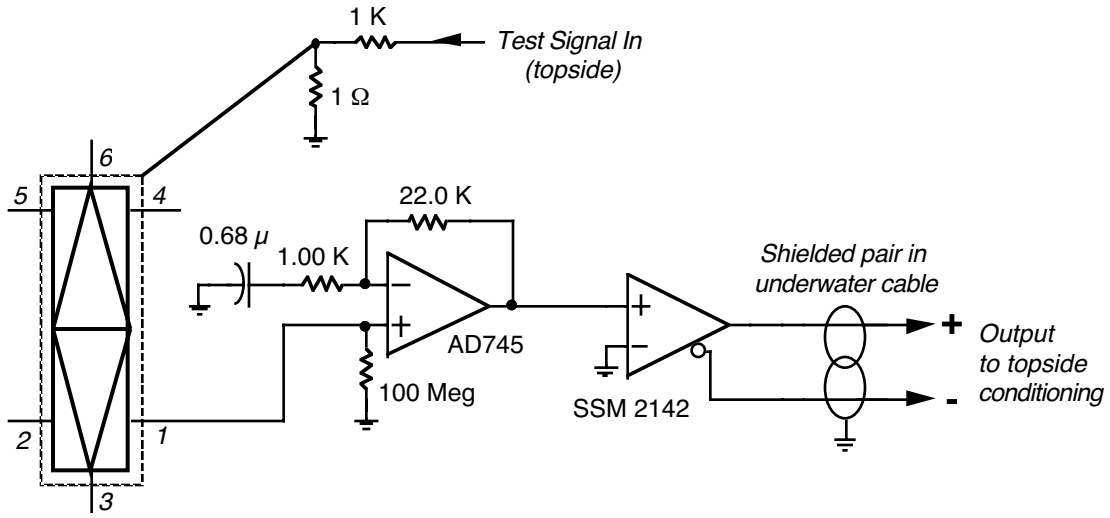

"Sandwich" Sensor Pickups With Local Ground.



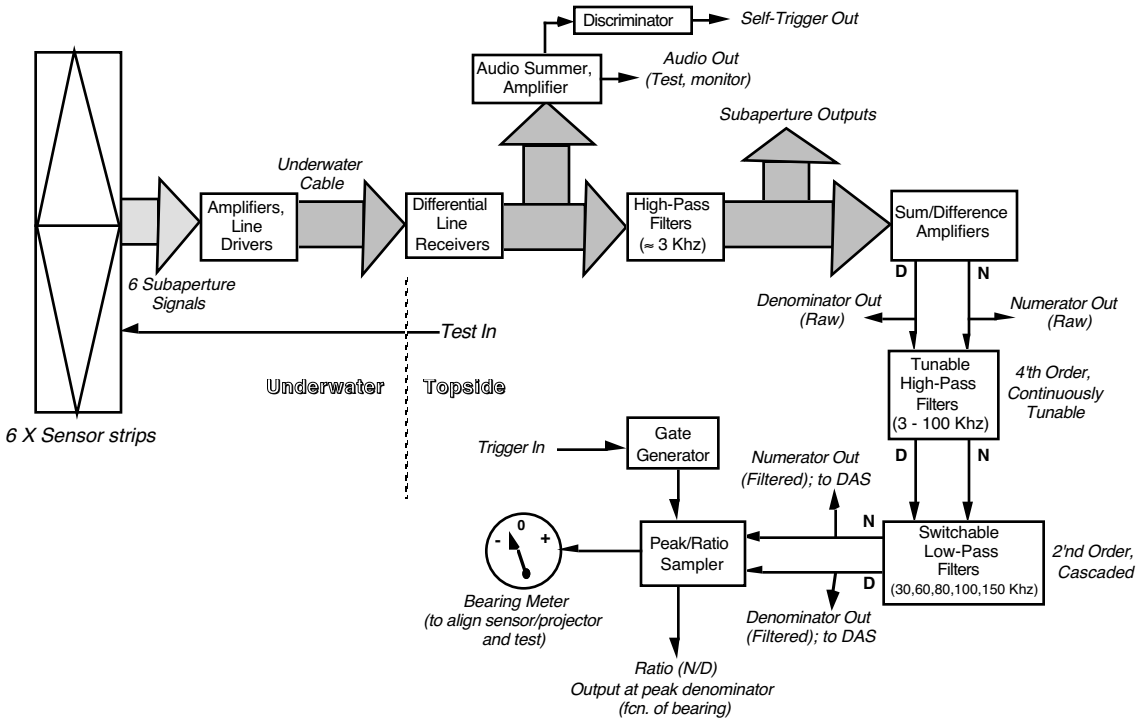

*3 Circuits per card*

# PC Design for New Front-End Amplifiers

3) **Final Version of the Prototype Electronics**




*a) Front-end electronics at sensor stave*




*b) Block diagram of signal conditioning system*

**Figure 6: Electronics for testing wideband monopulse prototypes**

Fig. 6 depicts the electronics that were developed to test the wideband monopulse stave described above. Fig. 6a shows the front-end amplifier that buffers each of the 6 subaperture outputs. This consists of a non-inverting gain stage designed around a low-noise JFET operational amplifier, followed by a unity-gain differential line driver that sends the subaperture signal across a

shielded 600 Ω pair to the topside electronics portrayed in Fig. 6b. The gain stage exhibits a high-pass response in order to attenuate noise from mechanical disturbances and PVDF thermal response; it provides a gain of 27 dB for frequencies above 200 Hz, rolling off to unity at DC. The front-end of Fig. 6a has been realized on two small 3-channel circuit cards, mounted in a watertight compartment directly behind the sensor stave. In order to improve shielding, a copper ground plane is laminated behind the subarpeture electrodes. The common plated surface of the PVDF is floated slightly from ground to allow a signal to be capacitively coupled into all subarpeture electrodes for test and calibration purposes.

Fig. 6b shows the corresponding topside signal conditioning electronics. The outputs from the front-end are differentially received, further amplified, then rolled off by a bank of second-order high-pass filters with cutoff at 3 kHz, again to attenuate mechanical noise and generic background from harbor activity (before filtering, these signals are summed, then provided to an audio tap for diagnostic monitoring and to an adjustable discriminator for self-triggering). The 6 filter outputs are then appropriately summed and differenced (as depicted in Fig. 6) to form numerator ($s_1$) and denominator ($s_0$) signals. Unwanted background is attenuated by adjusting a tracking pair of parametric high-pass filters (based around a 4'th-order CEM 3320 VCF) and selecting an appropriate low-pass rolloff, as listed in Fig. 6b. The filtered numerator (N) and denominator (D) signals are then digitized and stored by a Macintosh-based data acquisition system. After correcting for the 90° phase difference with an all-pass filter, these outputs are also directed to a circuit that latches the N and D signals at the peak D value over a gated interval (to minimize the scale errors from noise), then takes the analog ratio (N/D) to provide a coarse bearing indicator that is useful during system setup and adjustment, as discussed below.

The electronics shown in Fig. 6 were designed to provide maximum flexibility during the prototype tests. Production designs can be much simpler; i.e. the front-end plus sum and differencing can be realized with microchips mounted directly on the edges of the sensor stave, occupying minimal volume. The resulting pair of N and D signals can be digitized directly with minimal filtering, allowing further signal processing and analysis to be realized entirely in software. The addition of a time-varying gain (TVG) stage will maximize the dynamic range of the digitized signal.

Indeed, this set of electronics was built and used many times in Backgammon system tests. The following figures are layout diagrams by Rick Ciliberto, who fabricated the final topside unit and designed the panels. The first figure in this series shows the way the Backgammon electronics were wired together. This system was designed for two such sensor staves, with an underwater cable changing out to a DB25 cable in a cable "interface box", which plugged into the signal conditioning electronics (the front end amps and differential line drivers were all mounted on the staves themselves). The next figure shows the layout of the topside box, with connectors at rear and electronics card in back. The next figure shows Rick's wonderfully aesthetic design for the front panel on the conditioning electronics. The next figure is a photograph of the actual device,

followed by a photo of the rear of the device, open to show the electronics contained within (unfortunately, Rick wirewrapped the analog electronics card, but with a bit of careful rerouting and shielding, we were able to keep pickup and cross-coupling interference manageable).

7/17/92
R. Ciliberto

JOE
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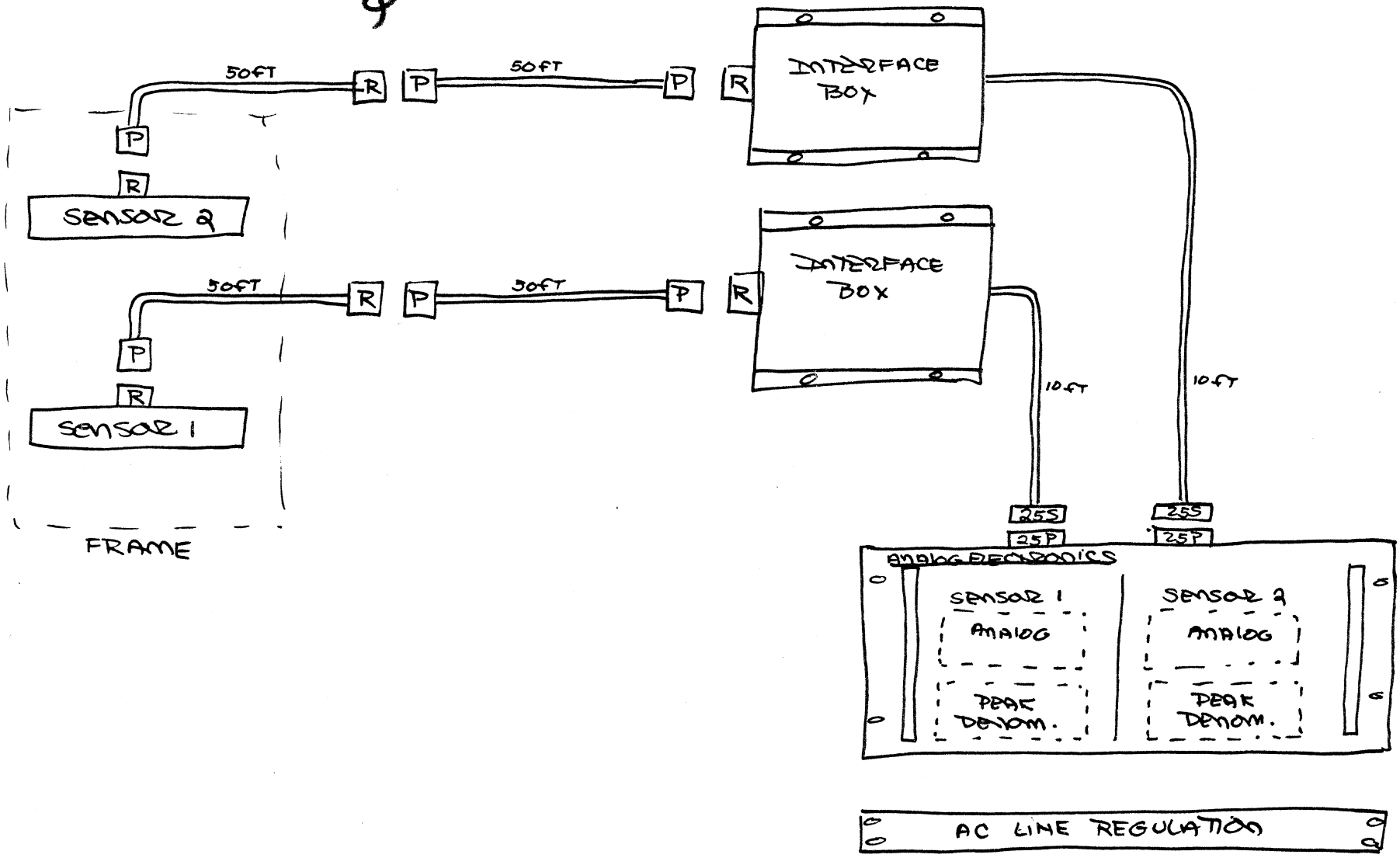
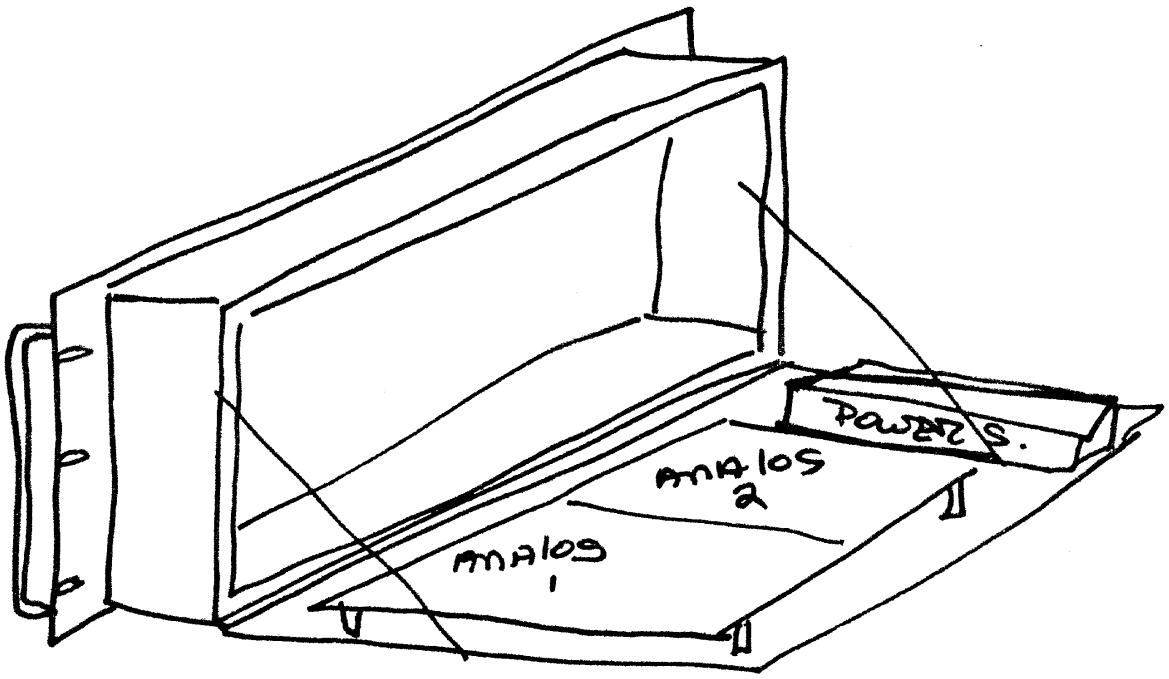
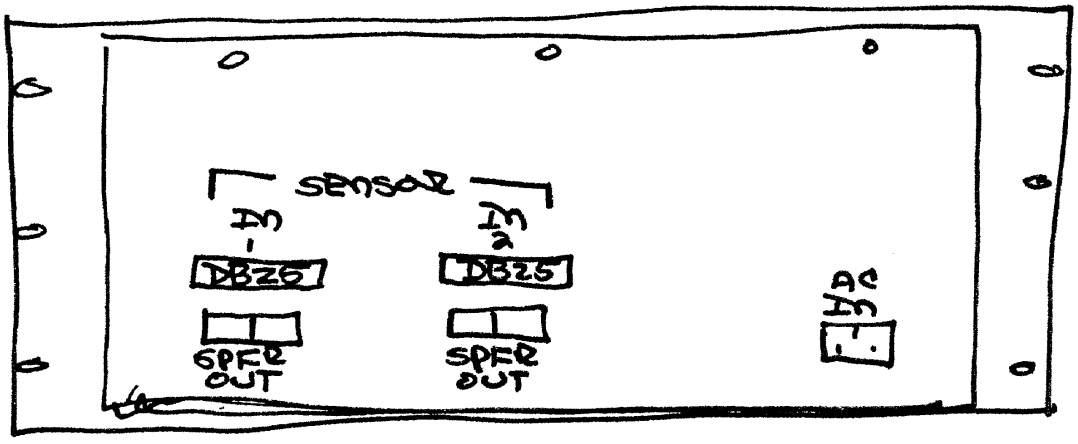



POWER S.
ANALOG 2
ANALOG 1


SENSOR
IN 1
IN 2
DBZ0
DBZ5
SPEC OUT
SPEC OUT
FAN

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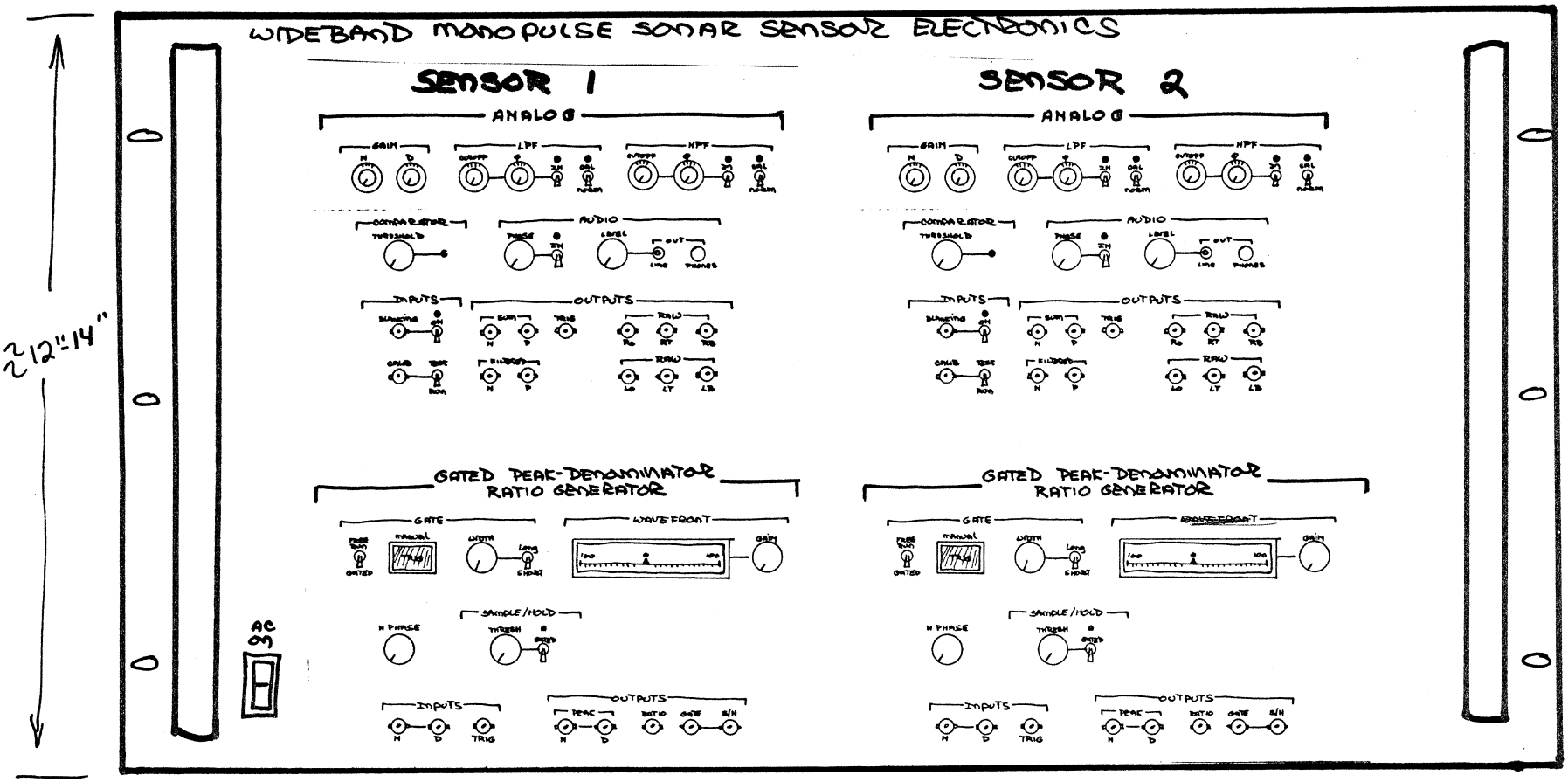
R. Ciliberto




SENSOR 1
SENSOR 2
BEARING
D-C MICROAMPERES
MAN TRIG
FREE RUN
GATED
WIDTH
LONG
SHORT
SCALE
S/H
THRESH
N PHASE
INPUTS
OUTPUTS
PEAK
RATIO
GATE
GAIN
COMPARATOR
AUDIO
LEVEL
LINE
PHONES
HPF
LPF
CUTOFF
FILTERED OUT
BLANKING
CALIB
SUM
SUBAPERTURE